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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,788	07/21/2003	Leonard Forbes	1303.109US1	6087

21186 7590 03/29/2007

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	PAPER NUMBER
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,788	FORBES ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-27,31-38 and 47-52* is/are allowed.

6)☒ Claim(s) *1-7,9-14,16-21,28,29,39-41,43-46 and 53* is/are rejected.

7)☒ Claim(s) *8,15,30 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/26/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the request for reconsideration on 26 December 2006. Claims 1-53 are pending; claims 54-65 have been previously cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 12, 16 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Clingman et al. (6,994,762).

Referring to claims 1 and 16, Clingman et al. disclose a method for forming a wafer where a predetermined contour is formed in one of a semiconductor membrane (12) and a substrate wafer (14); and bonding the semiconductor membrane (12) to the substrate wafer (14) and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane (12) (Fig. 1-3; col. 2, lines 61-66; col. 3, lines 44-64).

Referring to claim 2, wherein the predetermined contour is straightened when the semiconductor membrane is bonded to the substrate wafer (col. 3, lines 44-64).

Referring to claim 3, wherein the semiconductor membrane is bonded to the substrate wafer before the predetermined contour is straightened (col. 3, lines 32-43).

Referring to claim 6, wherein forming a predetermined contour in one of a semiconductor membrane and a substrate wafer includes applying a pressure to flex the substrate wafer to have a predetermined strain; and bonding the semiconductor membrane to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane includes: bonding a periphery of the membrane to a periphery of the substrate wafer; and removing the pressure to relax the substrate wafer and transfer strain from the substrate wafer to the semiconductor membrane (col. 3, lines 16-64).

Referring to claims 12 and 18, wherein the substrate wafer is glass (col. 2, line 66 thru col. 3, line 4).

Claims 28 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Belford (6,514,836).

Referring to claim 28, Belford discloses a method for forming a wafer where a central region of a substrate wafer (206) is flexed; performing a bond cut (smart cut) process to form a silicon membrane from a crystalline sacrificial wafer, bonding a peripheral region of the substrate wafer (206) to a peripheral region of a silicon membrane (202) when the substrate wafer (206) is in the flexed position; relaxing the substrate wafer (206) to induce a predetermined strain in the silicon membrane (Fig. 2; col. 3, lines 18-33 & 63-67). Wherein, applicant describes the bond cut technique

implants ions such as hydrogen, bonds two wafer surfaces together, and separates the two bonded wafers along the region of hydrogen implantation.

Referring to claim 29, defining the silicon membrane in a surface layer of a sacrificial crystalline silicon wafer; bonding the surface layer of the sacrificial wafer to the peripheral region of the substrate heat-treating the sacrificial wafer and the substrate wafer; and separating the sacrificial wafer from the membrane such that the silicon membrane remains strongly bonded to the substrate wafer (col. 3, lines 61-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 9-11, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clingman et al. in view of Belford.

Clingman et al. disclose the subject matter claimed above except performing a bond cut process, the membrane comprising silicon, the substrate comprising crystalline ad polishing the bonded crystalline wafer to thin the crystalline wafer and control the induced strain.

Referring to claims 4, 9 and 11, Belford discloses a method for forming a wafer where a central region of a substrate wafer (206) is flexed; performing a bond cut (smart cut) process to form a silicon membrane from a crystalline sacrificial wafer, bonding a

peripheral region of the substrate wafer (206) to a peripheral region of a silicon membrane (202) when the substrate wafer (206) is in the flexed position; relaxing the substrate wafer (206) to induce a predetermined strain in the silicon membrane (Fig. 2; col. 3, lines 18-33 & 63-67).

Referring to claim 7, Belford discloses applying a pressure to flex the substrate wafer to have a predetermined strain includes applying a pressure to a substrate wafer having a thickness sufficiently small such that the substrate wafer is flexible (col. 3, lines 6-32).

Referring to claims 10 and 43, Belford discloses polishing the bonded crystalline wafer to thin the crystalline wafer and control the induced strain (Fig. 2; col. 3, lines 63-65).

Referring to claims 13 and 17, Belford discloses the semiconductor membrane includes an ultra-thin semiconductor layer (col. 3, lines 16-33).

Referring to claim 14, Belford discloses the semiconductor membrane is between approximately 10 microns (col. 3. lines 25-29).

Since Clingman et al. and Belford are both from the same field of endeavor, a method for forming a wafer, the purpose disclosed by Belford would have been recognized in the pertinent art of Clingman et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Clingman et al. by performing a bond cut process as taught by Belford to reduce the short channel effects (col. 1, lines 45-63).

Referring to claims 19 and 20, Clingman et al. does not disclose the strain between 0.75% and 1.5%. It would have been obvious to one having ordinary skill in the art at the time invention was made to have a predetermined strain between 0.75% and 1.5% disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Claims 5, 21, 39-41, 44-46 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clingman et al. in view of Belford and Yamazaki et al. (6,902,616).

Clingman et al. and Belford disclose the subject matter above except wherein upon bonding, the semiconductor membrane and the substrate wafer forms a composite structure, the method further comprising bonding the composite structure to a carrier substrate.

Referring to claims 5, 21 and 39, Yamazaki et al. disclose a method for forming a wafer including a convex contour in a surface of a sacrificial crystalline wafer; and bond a ultra-thin semiconductor membrane to a substrate wafer, wherein the ultra-thin semiconductor membrane is flattened and strained when bonded to the substrate wafer, wherein upon bonding, the semiconductor membrane and the substrate wafer form a composite structure, the method further comprising bonding the composite structure to a carrier substrate (Fig. 6A-7C; col. 5, lines 46-61).

Since Clingman et al. and Yamazaki et al. are both from the same field of endeavor, a method for forming a wafer, the purpose disclosed by Yamazaki et al.

would have been recognized in the pertinent art of Clingman et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Clingman et al. by upon bonding, the semiconductor membrane and the substrate wafer form a composite structure, the method further comprising bonding the composite structure to a carrier substrate as taught by Yamazaki et al. to increase threshold voltage (col. 2, lines 8-34).

Referring to claim 40, Belford discloses the semiconductor membrane includes an ultra-thin semiconductor layer (col. 3, lines 16-33).

Referring to claim 41, Yamazaki et al. disclose heat-treating the sacrificial wafer and the substrate wafer; and separating the sacrificial wafer from the membrane such that the silicon membrane remains strongly bonded to the substrate wafer (col. 3, lines 30-34).

Referring to claims 44 and 53, Yamazaki et al. disclose forming a gate separated from the strained semiconductor layer by a gate insulator; and forming first and second diffusion regions separated by a channel region, the strained semiconductor layer including the first and second diffusion region and the channel region (col. 4, lines 1-5). Although Yamazaki et al. does not specifically disclose forming a gate separated from the strained semiconductor layer by a gate insulator; first and second diffusion regions separated by a channel region they are inherent features in the formation of a thin film transistor.

Referring to claims 45 and 46, Belford discloses a method for forming a wafer where a central region of a substrate wafer (206) is flexed; performing a bond cut (smart

cut) process to form a silicon membrane from a crystalline sacrificial wafer, bonding a peripheral region of the substrate wafer (206) to a peripheral region of a silicon membrane (202) when the substrate wafer (206) is in the flexed position; relaxing the substrate wafer (206) to induce a predetermined strain in the silicon membrane, wherein the semiconductor layer is wafer sized (Fig. 2; col. 3, lines 18-33 & 63-67).

Allowable Subject Matter

Claims 22-27, 31-38 and 47-52 are allowed.

Claims 8, 15, 30 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Referring to claims 8, 15, 30-38 and 42, prior art does not anticipate, teach, or suggest forming voids in the substrate wafer to provide the substrate with a desired flexibility.

Referring to claims 22-27 and 47-52, prior art does not anticipate, teach, or suggest bonding a peripheral region of the substrate wafer to a peripheral region of a silicon membrane and not bonding the silicon membrane to the central region of the substrate wafer when the substrate wafer is in the flexed position.

Response to Arguments

Applicant's arguments filed 26 December 2006 have been fully considered but they are not persuasive. As stated above, Clingman et al. disclose the method for

forming a wafer as described in claim 1 and Belford discloses the method for forming a wafer as described in claim 28.

In response to the applicant's arguments, the applicant argues Clingman et al. do not teach bonding a semiconductor membrane to a substrate wafer, rather a steel layer. However, in column 2 at line 65, Clingman et al. teach the steel layer (14) may be a substrate. Applicant also argues Belford does not teach performing a bond cut to a flexed region of a substrate. However, Belford discloses a strained region, in it broadest interpretation, flexing a region creates strain. Belford discloses using the bond cut (smart cut) to a strained silicon on insulator, applicant claims a method for forming a wafer, this may include a silicon-on-insulator wafer. During patent examination, the claims are given the broadest reasonable interpretation consistent with the specification. See *In re Morris*, 127 F.3d 1048, 44 USPQ2d 1023 (Fed. Cir. 1997). See MPEP § 2111 - § 2116.01 for case law pertinent to claim analysis.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP
21 March 2007

Zandra V. Smith
Supervisory Patent Examiner
On March 2007